

# High-speed digital acquisition system based on FPGA

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**Abstract.** Data acquisition system is widely used in modern technology. This paper designs a high-speed digital acquisition system based on FPGA. In the design, the FPGA is the core of the control system, control of high speed ADC sampling data, and combining the Altera company's FIR low-pass filtering IP check out data, and convert the data throw the FIFO, and the data stored in a dynamic memory SDRAM, and turn the USB serial port circuit transmission to the computer display and data analysis. The reliability of the system was verified by MATLAB processing.

## 1. Introduction

With the development of science and technology, data acquisition system has been widely used in more and more fields, such as industrial control, wireless communication, scientific experiment and other fields. At present, the common high-speed data acquisition card in the market is the ISA card or PCI card, the general price is expensive, the installation is inconvenient, and the internal storage speed is slow, which is not conducive to the expansion of development design. The existing high-speed data acquisition card has not been able to meet the requirements of modern science and technology, and it needs more rapid and reliable collection system. Based on the design principles of economy, practicality, simplicity, reliability and safety, this paper proposes a design scheme of data acquisition system based on FPGA which is high speed, high accuracy and low power consumption.

## 2. Basic theory of data collection

Data acquisition refers to the automatic collection of non-electricity or power signals from sensors and other test equipment and other analog and digital devices to carry out the analysis and processing of the upper computer.

Suppose you take a sample signal  $x(t)$  every  $\Delta t$  time. The time interval  $\Delta t$  are called sampling intervals or sampling cycles. Its inverse  $1/\Delta t$  is called the sampling frequency, and the unit is the number of samples per second. For the time is  $t = 0, 1, \Delta t, 2\Delta t, \dots$  and so on. The value of  $x(t)$  is the sample value. All the value of  $x(0)$ ,  $x(\Delta t)$ ,  $x(2\Delta t)$  are sample values. According to the sampling theorem, the lowest sampling frequency must be twice the signal frequency. On the other hand, if a sampling frequency is given, the maximum frequency that can correctly display the signal without distortion is called the Nyquist frequency, which is half the sampling frequency. If the signal contains frequencies higher than the Nyquist frequency, the signal will be distorted between the dc and the Nyquist frequencies.

## 3. Systematic design

In this design based on FPGA as the main core device, control of high speed ADC sampling data, using Altera corporation provide FIR low-pass filtering IP check out data, and the temporary data

exist in the SDRAM memory after filtering, after turn the USB serial port circuit transmission to display on a computer, finally combining with the Matlab software to collect data for analysis. The signal sampling process is shown in figure 1.

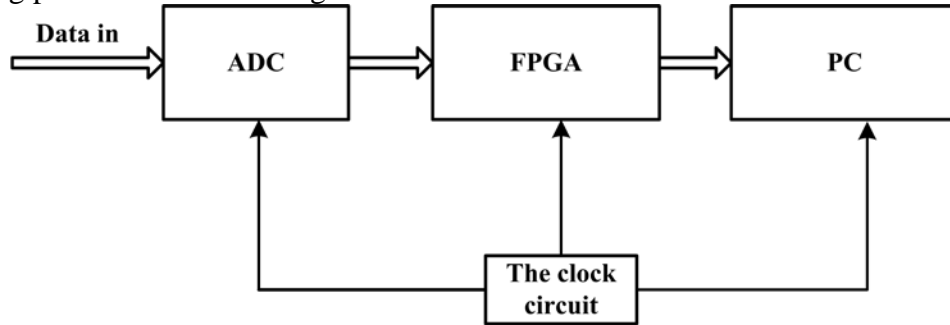


Figure 1 signal sampling process

The design mainly includes A/D sampling module, FIR digital filtering module, FPGA control module, SDRAM storage module, and USB switch serial port circuit.

### 3.1. ADC

The main function of digital-to-analog converter (ADC) is to convert analog signals into digital signals. The chip used in this module is a high-speed AD/DA module launched by the black gold dynamic community. The module consists of two kinds of chips: AD and DA. The sampling rate is fast and the accuracy is high, which is suitable for the high-speed acquisition system.

AD circuit of the module is made up of high speed AD chip, attenuation circuit and signal input interface, including high speed AD chip is introduced by the AD company eight, maximum sampling rate 32 AD9280 chip installed base, the AD chip input range (0 ~ 2 v). Its internal structure is shown in figure 2.

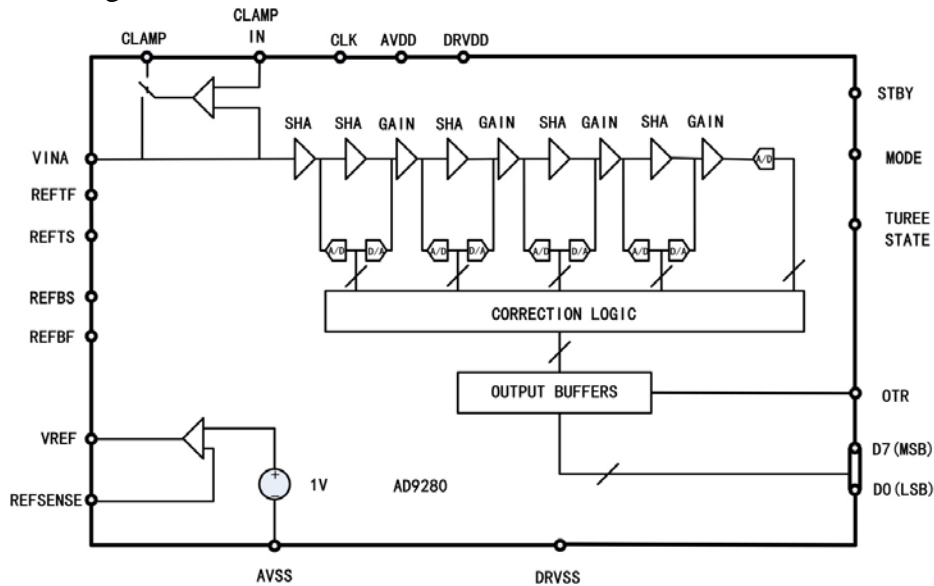


Figure 2 internal structure of AD9280 chip

The input range of the AD/DA module is -5v ~+5V (10Vpp), but the input voltage range of the AD9280 chip is (0 ~ 2V). So in order to satisfy the voltage range of the input signal, the signal into AD chip before, first with a piece of AD8056 chips built attenuation circuit, attenuation after input range to meet the AD chip input range (0 ~ 2 V), according to the figure 3 will AD voltage input range is set to 0 ~ 2 V.

Therefore, before the signal enters the AD chip, the attenuation circuit is constructed with a piece of AD8056 chip, which meets the input range of the AD chip (0 ~ 2V), and the transformation formula is as follows:



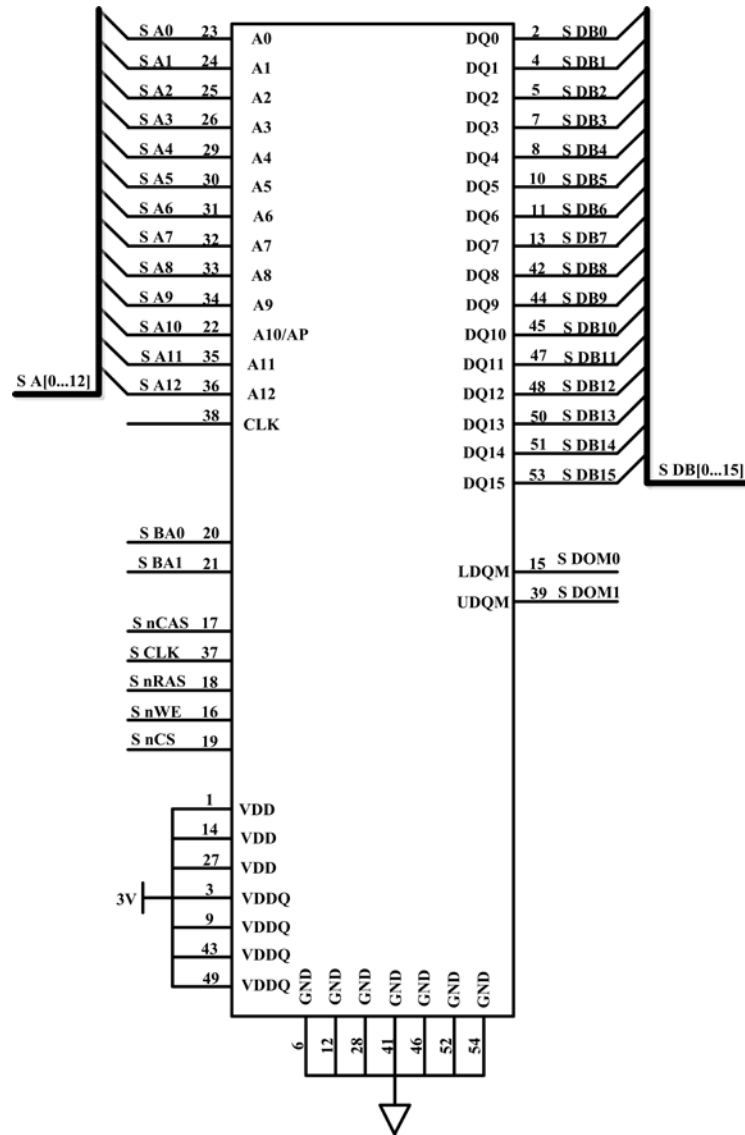


Figure 5 SDRAM peripheral interface circuit diagram

### 3.3. The FPGA module

The FPGA system is the core of the data acquisition system, to realize the collection of the signal and control operations such as reading and writing, has the rich logical unit and I/O interface resources, is a highly integrated chips, with internal delay of small, high efficiency, easy to expand, I/O resources are rich, diverse storage, etc.

This is used in the design of FPGA development board Cyclone III EP3C16F484C series.

There are two main functions. One is to generate the clock frequency of the system ADC module, and the other is the acquisition of signal. The maximum sampling frequency of the digital converter is 32 MSPS, the clock frequency of SDRAM is 200 MHZ, because the FPGA system's crystal frequency is 50 MHZ, in order to achieve the highest sampling rate of ADC, using FPGA within the PLL (Phase Locked Loop and phase-locked Loop) by frequency division, frequency doubling or shift needed to implement the modules such as clock frequency.

FPGA acquisition signal work process is: through the signal attenuation circuit under test signal attenuation to the A/D chip input voltage range, adjust clock frequency control by FPGA system sampling A/D chip, the A/D chip output signal input to the acquisition of the FPGA system, finally the FPGA system through the USB serial port in the circuit the signal input to the host system for processing.

#### 4. Implementation of system design

The systems uses the hardware description language Verilog HDL as programming language, through the Quartus II software for FPGA system programming, and write the Testbench test program, combining with ModelSim software simulation test platform of simulation test on the parts.

In order to analyze the accuracy of the sampled data, the data collected is analyzed by MATLAB software.

To collect frequency of 1 MHz, 3V by sine wave signal as an example, the sampling frequency is 32 MHz, serial interface circuit through the USB to upload hexadecimal data, and save it to the TXT text document, for the follow-up of signal analysis and processing. Figure 6 is the result of the experiment

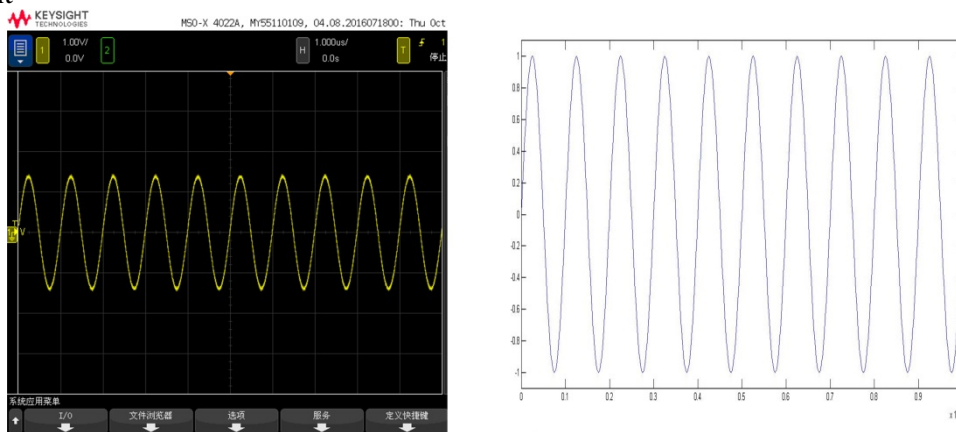


Fig 6 the result of the experiment

The simulation results show that the design is correct.

#### 5. Conclusion

The maximum sampling rate of the FPGA based high-speed acquisition system can reach 32MSPS. The acquisition system has the advantages of fast sampling rate, high accuracy and high universality, and can adjust the number of sensors, channel number, sampling bandwidth and strong universality.

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